DESIGN FOR MANUFACTURABILITY

ASIC design flow considering lithography-induced effects

K. Cao and J. Hu

Abstract: As VLSI technology scales towards 65 nm and beyond, both timing and power performance of integrated circuits are increasingly affected by process variations. In practice, people often treat systematic components of the variations, which are generally traceable according to process models, in the same way as random variations in process corner-based methodologies. In particular, lithography-induced process variations are usually estimated by a universal worst-case value without considering their layout environment. Consequently, the process corner models based on such estimation are unnecessarily pessimistic. A new ASIC design methodology that captures lithography-induced polysilicon gate length variations including both the layout dependent systematic components and random components is proposed. This methodology also shows that lookup table methodology is sufficient to handle back end of line lithography process variations in timing analysis. In addition, a new technique of dummy poly insertion is suggested to shield inter-cell optical interferences. This technique together with standard cells characterised using the new methodology will let current design flows comprehend the variations almost without any changes. More importantly, by separating systematic lithography effect from random process variations, this methodology greatly reduces pessimism in timing analysis, thus enabling both aggressive design implementation and easier timing signoff. Experimental results on industrial designs indicate that the new methodology can averagely reduce timing variation window by 11% and power variation window by 55% when compared with a worst-case approach.

1 Introduction

The International Technology Roadmap for Semiconductors projects that process variations present a critical challenge for both manufacturing yield and parametric yield of integrated circuit products. The process variations consist of systematic components and random components. The systematic variations represent both front end of line (FEOL) and back end of line (BEOL) parameter variations caused by predictable design and process procedures, such as critical dimension (CD) variations from different poly gate pitches and metal thickness variations occurred during chemical mechanical planarisation. Therefore systematic variations behave deterministically in general.

In many existing design methodologies, people usually treat systematic variations together with random variations without differentiation. By handling both kinds of variations together in a process corner-based methodology, people can conveniently circumvent relatively complex systematic variation models. However, such simplification usually causes unnecessary pessimism in process corner estimations especially when the systematic components account for a large portion of the overall variations. Indeed, it is reported in [1] that more than 50% of transistor gate length variations are due to systematic sources. As VLSI technology aggressively scales to 65 nm and beyond, the influences from both systematic and random variations become greater and greater. The consequently expanding process corners force designers to set aggressive timing targets which intensify both design productivity crisis and power crisis [2]. Therefore significant pessimism in process corner estimations is no longer tolerable and systematic variations need to considered differently from random variations.

Among systematic variations, transistor gate length variation has perhaps the largest impact on circuit timing and power performance since it directly affects both transistor switching speed and leakage power. Fortunately, gate length variation largely depends on lithography process and can be captured through lithography/optical proximity correction (OPC) simulation. A pioneer work [3] tried to estimate gate length variations through computationally expensive aerial image process simulations. Recently, a post-OPC extraction methodology was proposed [4] for timing analysis of critical paths in a design. In [4], it is found that timing critical paths are changed when post-OPC extraction information is utilised. However, the overall timing performance of a circuit is not altered by this methodology. Another work [5] proposed a timing analysis methodology with awareness of lithography-induced gate length variations according to different poly pitches. For a standard cell, three poly spacing ranges are considered for its four boundaries and thereby 81 variants are characterised for each cell. The timing characteristic of a cell instance in a layout is obtained by matching its surrounding layout pattern with one of the 81 variants.

In [6], we presented a new standard cell characterisation methodology considering lithography effects. In this paper,
we extend this discussion into BEOL to investigate the timing impact of lithography effects on routing metals. We then present a new litho-aware timing analysis flow which considers lithography-induced effects on both gate length variations and interconnect wire-width variations. In this methodology, the timing and power performance of a cell is based on layout shapes obtained from lithography and OPC simulations and the interconnect wire-width variations is considered with a lookup table. The main contributions in our work are as follows.

- A new technique of dummy poly insertion is suggested to handle the dependence of gate length variations on inter-cell spacing. In general, the gate length variations in the boundary regions of a cell depends on its spacing with out-skirt poly of neighbouring cells. However, the neighbouring cell information is not available before cell placement is completed. Our dummy poly insertion technique can generally avoid such dependence on unknown information. Therefore we do not need to characterise different variants of a cell as in [5]. Moreover, we do not have to perform the pattern matching-based variant selection as described in [5] in later design stages. In other words, the lithography-aware cell characteristics can be utilised without affecting current standard cell-based design flows.
- We utilise a poly segmentation technique similar to that in [7, 8] to accurately evaluate arbitrarily irregular poly shapes. The printed poly shapes on wafer not only have deviations on gate length, but also have different deviations on different spots of a same poly. In other words, the deviations are by and large non-uniform. Our approach is in contrast to many previous works which treat the deviation of a poly uniformly.
- We verified that for lithography effect on wire width of interconnect, traditional lookup table method is still valid.

Accurate lithography simulations, including OPC, photo-resist and etch simulations, are time consuming in general. For practical design use in timing analysis, it is thus very difficult to run lithography simulations on the full chip level. However, the size of a library cell is very small and the characterisation is usually performed only once. Therefore the expensive lithography/OPC simulation are affordable in this scenario. More importantly, cell-based timing annotation methodology is used in typical timing analysis for standard cell-based application-specific integrated circuit (ASIC) design. In order not to disturb this flow, it is therefore very desirable for a methodology to capture lithography effect in a cell-based fashion. Traditional ASIC static timing analysis (STA) flow utilises process corner conditions for timing signoff. This approach introduced high level of pessimism. For example, in slow process corner, all transistor gates are assumed to have the largest gate lengths. In reality, this will never happen. Because of the systematic nature for lithography effects, our methodology predicts this portion of the variations and take it into consideration for STA to reduce pessimism significantly. We applied our methodology to industrial library cell designs. The experimental results indicate that our methodology can averagely reduce timing variation window by 11% and power variation window by 55% when compared with an existing approach.

2 Overview of methodology

2.1 FEOL lithography variations

2.1.1 Standard cell architecture: It is claimed in [4] that litho simulation on individual standard cell does not represent accurate lithographic effect for that standard cell in block-level designs because lithographic effect depends on proximity of that standard cell. However, increasing the distance between one shape and the other will reduce the impact of the lithographic effect of other shapes tremendously. It is also very important to note that the closest neighbours of a shape are the dominating factors to model-based OPC process and sub-resolution assist features (SRAFs) generation for a particular shape.

We ran Mentor Graphics Calibre LFD on two sets of test structures shown in Fig. 1. The first set of the structures have three shapes with distance \( L \) between them. The second set of structures have five shapes where the distance between the middle shape and the shapes on both sides is also \( L \). The shapes next to the middle shape are \( L_1 \) away from it. In both sets, \( L \) is changing and \( L_1 \) in second set is fixed. The CD data for the middle shape are recorded from our lithography simulation tool.

The result is shown in Fig. 2. We can see that the CD of test structure 2 has much less variations than that of test structure 1, that is, having neighbouring shapes with a fixed distance really helps reducing printability variations of that shape. Also, other test structures we ran showed that a shape has minimal impact on another shape’s printing image if there are two or more shapes between them.

The range of \( L \) and \( L_1 \) that we chose to exercise the test structures is hardly random. In our 65 nm standard cell library implementation, \( L \) is the range of the possible poly gate spacing if two standard cells are placed adjacent to each other. If the two neighbour cells have gate space larger than \( L \), a filler cell with a dummy poly will be inserted between these two cells for design rule check (DRC) and power connectivity purposes. For the first set of test structures, we observe over 10% of CD variability over the range of \( L \). However, in our standard cell library architecture, we can put a dummy poly shape at the cell border
without introducing any area penalty. In this case, the value of $L_1$ in our test structures represents the minimum spacing between the dummy poly and active transistors in the standard cell. When two cells are placed side by side, the dummy poly shapes of both cells overlap exactly (Fig. 3). The dummy poly falls nicely in the gap of the diffusion areas between the two abutted standard cells, thus minimising the impact on the standard cell area. In fact, we processed an entire 65 nm production standard cell library without incurring any area penalty. We also would like to point out that the dummy poly shapes we insert are field poly, that is, they do not form new devices as they fall in the gap of the diffusions between two closely placed standard cells. Thus, these shapes do not cause extra layout versus schematic (LVS) verification efforts. Our standard cell designs ensure DRC of the dummy poly lines as the gap of the diffusion is large enough. By adding dummy poly shapes into the original standard cells, we introduce fixed closest neighbours to the poly gates that are at the cell boundary, thus greatly reducing the CD variations introduced by various proximities of this standard cell in the design as shown in Fig. 2. In fact, they effectively ‘shield’ all the internal transistors from lithographic effects of neighbouring structures.

2.1.2 Calculation of effective transistor with litho effects: In lithography process, there are several contributors of the poly gate length variations (Fig. 4). One of them is the variation caused by poly pitch to neighbours. The other is the L-shaped poly cornering effect, which is particularly important for small transistors. This effect is clearly shown in the middle transistor in Fig. 4. To obtain an accurate prediction of the transistor behaviour, we need to account for multiple sources of poly gate length variations.

The lithography-induced deviations of the critical dimension, which is the poly gate length, are usually in the order of a few nanometers. For other larger shapes, the relative shape deviation is much smaller. In a typical 65 nm design, poly gate width and diffusion dimensions are at least two or three times of the gate length. This means that lithography-induced circuit performance variations are mostly due to gate length deviation. It is therefore sufficient to extract the lithography information for only poly gate length. The printed image of gate poly shapes across process window will be employed to replace gate length image offset parameters introduced by traditional process corner models. We keep all the other process corner parameters unchanged, such as threshold voltage variation, gate oxide variation and so on.

After lithography/OPC simulations, we have an estimation of the printed images of poly shapes. Ideally, we wish to run SPICE simulations to obtain timing and leakage power profiles of the cell. However, current device models in SPICE can handle only rectangular-shaped transistors, whereas the lithography/OPC simulation results are often irregular shapes. For example, a gate length is relatively large at the location of a jog, but is small right before reaching that jogging region. In order to solve this mismatch, we try to compute an effective gate length which may provide the same timing/power performance of a post-lithography/OPC simulations poly shape. In general, the on current $I_{on}$ of a transistor determines the timing performance of this transistor. The leakage power of a transistor is mostly dependent on the off current $I_{off}$ of the transistor. Since on and off currents of a transistor usually have different sensitivities to gate length variations, we need to use different effective gate lengths for timing and leakage.

We utilise a segmentation technique to compute the effective gate length for timing and leakage. First, we construct two lookup tables for transistor $I_{on}$ and $I_{off}$. For both tables, each row corresponds to a specific transistor gate width and the columns are for different transistor gate lengths. Each entry of the table represents $I_{on}$ or $I_{off}$ of a transistor with gate width and length specified by the row and column indices. The ranges of transistor width and gate length, that is, the ranges of row and column indices, are based on typical transistor sizes allowed in fabrication. The values of $I_{on}$ and $I_{off}$ are obtained through SPICE simulations. Next, we chop a poly shape from lithography/OPC simulations into multiple segments and each segment can be approximated by a rectangle. This is illustrated in Fig. 5. The $I_{on}$ and $I_{off}$ of each small segment can be obtained from a simple calculation based on the lookup tables. Note that the width of a segment is usually much smaller than fabrication allowed size. Thus, it cannot be matched to any row index in the lookup tables. We suggest to solve this discrepancy through scaling. For example,
consider a transistor with nominal gate length 65 nm and width 200 nm. We chop its gate poly shape from lithography/OPC simulations into ten segments. Thus, each segment has a length \( l_i \) and width of 20 nm. Then, we can find the on current \( I_{on}(l_i, 200 \text{ nm}) \) from the lookup tables. The on current of this segment can be approximated as \( I_{on}(l_i, 20 \text{ nm}) = I_{on}(l_i, 200 \text{ nm})/10 \). The off current \( I_{off}(l_i, 20 \text{ nm}) \) can be calculated in the same way.

Once the on and off currents of all segments are available, the overall currents of the entire transistor based on the lithography/OPC simulated poly shape can be calculated as

\[
I_{on,\text{shape}} = \sum_{i=1}^{n} I_{on}(l_i, w) \\
I_{off,\text{shape}} = \sum_{i=1}^{n} I_{off}(l_i, w)
\]

where \( n \) is the number of segments and \( w \) the width of each segment.

Lastly, the effective gate length \( L_{eff,\text{timing}} \) can be found based on the estimated \( I_{on,\text{shape}} \) and the lookup table of on current. From the nominal transistor width, we can find its corresponding row in the lookup table. We search for the entry in the row with value closest to the \( I_{on,\text{shape}} \) obtained above. The column index for this entry is the \( L_{eff,\text{timing}} \) for this transistor. The effective length \( L_{eff,\text{leakage}} \) can be obtained in the same way based on \( I_{off,\text{shape}} \) and the lookup table for off current.

### 2.1.3 Netlist back annotation and standard cell characterization

After we calculate the effective gate length \( L_{eff,\text{timing}} \) and \( L_{eff,\text{leakage}} \) of each poly gate shape, we need to back annotate the standard cell SPICE netlist with these effective gate lengths. The layout of a transistor may consist of multiple fingers and lithography usually has different effects on each finger depending on the layout environment. Therefore, we need to treat these fingers separately even though they belong to the same transistor. When an LVS tool runs in its normal mode, it automatically merges multiple fingers of a transistor into a single gate. To avoid this merging, we perform a special LVS that takes the \( x \) and \( y \) coordinates of each poly gate shape into a layout netlist even when some poly gate shapes are the fingers of the same transistor. The layout netlist will be fed into our extraction tool to generate a netlist with parasitics. The extracted netlist also keeps each poly gate shape as a separated device. We then use the \( x \) and \( y \) coordinates to match the poly shape in the extracted netlist with poly shape contours from lithography/OPC simulations. We back annotate the \( L_{eff,\text{timing}} \) and \( L_{eff,\text{leakage}} \) into the extracted netlist. Thus, for each standard cell, we generate one netlist for timing simulation and another netlist for leakage power simulation. By including dose and focus variations in the lithography/OPC simulations, we can have the extracted netlist for each cell at the worst and the best process corners.

### 2.2 BEOL lithography variations

For interconnections, lithography also introduces variations, mainly on the width of the wire. In Fig. 6, we show the contour of the metal wire on top of the intended drawn shape. The distortion of the routing metal also introduces timing variations. Therefore, we will also need to consider these effects for STA. However, it is obviously true that metal shape distortions do not impact timing in a noticeable way locally in an individual standard cell because of the small size of the cells. For interconnection, signal routing is often done in a grid-based fashion, meaning that most portion of the wire will have stable and predictable environment. It is interesting to note that even though part of the interconnection will be distorted by lithography process significantly, the wire stays close to the drawn shape across most of its length. In this section, we will verify that traditional parasitic extraction methodology with a lookup table still applies for STA analysis considering lithography effects.

We compare the STA results from two different approaches, one with full lithography simulation on BEOL interconnection wire width and the other using lookup table extraction.

#### 2.2.1 Lithography simulation on BEOL

After performing lithography simulation on BEOL, we obtain the contour of the wire. However, the contour is presented by a polygon with a large number of vertexes. It would be extremely difficult for the extraction tool to handle these kinds of polygons. In order to solve this problem, we convert these polygons to smoother ones. This process is described as follows.

- We convert the polygon to a Manhattan polygon whose segments are either vertical or horizontal.
- We define a threshold value for wire width change between adjacent wire segments. If the change for adjacent edges is smaller, we merge the two segments into one with the average wire width for the segment, as shown in Fig. 7.
- We use the bounding box of the VIA shapes for VIA area.

#### 2.2.2 STA comparison

Two separate STAs are performed, one use drawn shape routing metal for extraction, and the other use polygons converted from litho contours.
of the routing metals. We verified that the timing difference is very minor. The results are presented in the experiment section.

2.3 Litho-aware STA flow

Based on our analysis of FEOL and BEOL litho effects, we conclude that we should focus most of the efforts on poly gate litho effects of standard cells for litho-aware timing analysis flow. With accurate litho simulation and device characterisation, we are able to extract timing impact of litho process for a given standard cell. At the same time, with an effective technique such as dummy poly insertion, we are able to minimise timing variation caused by standard cell context for a placed design. For BEOL routing metals, we show that we can continue to use current parasitic extraction methodology. In summary, the litho-aware timing analysis flow will reduce the pessimism of the traditional corner-based signoff methodology. At the same time, the evolution to the litho-aware timing analysis flow from the current STA flow mostly happens in the standard cell development and characterisation. The costly litho simulations can be avoided in the block and chip levels.

3 Experiment

3.1 Standard cells

We follow the flow shown in Fig. 8 for standard cell characterisation. From the original standard cell, we first insert dummy poly on the boundary of the standard cells, we stream out the GDS to feed into our litho simulation tool. We then use the result of the litho simulation to generate the new netlist with the lookup table for timing and leakage. Lastly, we run the standard cell characterisation with our standard flow and tools.

![Fig. 8 Litho-aware standard cell characterisation flow](image)

![Fig. 9 Lithography-induced Lgate deviation distribution: worst corner](image)

![Fig. 10 Lithography-induced Lgate deviation distribution: best corner](image)

Table 1: Experimental results for standard cell characterisation

<table>
<thead>
<tr>
<th>Cell</th>
<th>Original timing variation, ps</th>
<th>New timing variation, ps</th>
<th>%</th>
<th>Original leakage ratio</th>
<th>New leakage ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>inv</td>
<td>142.0</td>
<td>127.4</td>
<td>10.3</td>
<td>16.5</td>
<td>9.8</td>
</tr>
<tr>
<td>and2</td>
<td>268.2</td>
<td>243.2</td>
<td>9.3</td>
<td>24.5</td>
<td>11.4</td>
</tr>
<tr>
<td>or2</td>
<td>203.9</td>
<td>182.9</td>
<td>10.3</td>
<td>15.8</td>
<td>7.2</td>
</tr>
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<td>104.4</td>
<td>11.1</td>
<td>14.1</td>
<td>6.1</td>
</tr>
<tr>
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<td>119.3</td>
<td>105.7</td>
<td>11.4</td>
<td>14.9</td>
<td>6.4</td>
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<td>268.8</td>
<td>11.7</td>
<td>15.9</td>
<td>6.3</td>
</tr>
<tr>
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<td>361.3</td>
<td>8.3</td>
<td>27.8</td>
<td>13.4</td>
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<tr>
<td>oai211</td>
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<td>159.8</td>
<td>9.7</td>
<td>13.7</td>
<td>7.0</td>
</tr>
<tr>
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<td>155.2</td>
<td>8.4</td>
<td>15.3</td>
<td>7.0</td>
</tr>
<tr>
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<td>270.0</td>
<td>25.2</td>
<td>20.3</td>
<td>8.4</td>
</tr>
<tr>
<td>ao21</td>
<td>211.3</td>
<td>189.6</td>
<td>10.3</td>
<td>16.5</td>
<td>6.5</td>
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<tr>
<td>buffer</td>
<td>228.2</td>
<td>203.4</td>
<td>10.9</td>
<td>21.0</td>
<td>8.0</td>
</tr>
<tr>
<td>ha</td>
<td>303.2</td>
<td>273.6</td>
<td>9.8</td>
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<td>7.6</td>
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<tr>
<td>mux</td>
<td>238.3</td>
<td>211.2</td>
<td>11.4</td>
<td>17.2</td>
<td>8.1</td>
</tr>
<tr>
<td>oai21</td>
<td>254.6</td>
<td>223.4</td>
<td>12.3</td>
<td>17.3</td>
<td>7.3</td>
</tr>
<tr>
<td>ave</td>
<td>232.8</td>
<td>205.3</td>
<td>11.4</td>
<td>17.8</td>
<td>8.0</td>
</tr>
</tbody>
</table>
corner, which has the worst RC parasitic extraction, we change the length of each gate to the longest $L_{\text{eff}}$ of that specific gate, this gives us the annotated cell netlist at the worst timing corner. We do the same for original cell netlist the at the best timing corner except that we use the shortest $L_{\text{eff}}$ of each gate to replace the original gate length in the netlist and we obtain the annotated cell netlist at the best timing corner. We repeat the process for leakage corners and obtain the annotated cell netlists at the best and worst leakage corners.

In Figs. 9 and 10, we show the distributions of lithography-induced gate length deviation for both best and worst timing corners for all our library cells. The $y$-axis in Figs. 9 and 10 are the difference between $L_{\text{eff}}$ of that gate and the draw length, and the $y$-axis are the number of poly transistor gates with the specified gate length deviation. We show that gate length variations can be as much as 16 nm across process window. Although the data reveals the level of immaturity for current 65 nm resolution enhancement techniques including OPC and SRAF generation, it further confirms the value of our methodology which considers lithography-induced gate length variations in a systematic fashion.

All the generated netlists have been characterised with our standard cell characterisation flow. We present the timing and leakage variabilities of a set of representative standard cells in Table 1. In columns 2 and 3, we report the timing variation between the two timing signoff corners with the original standard cell netlist and with our new netlist, and the percentage change is reported in column 4. In columns 5 and 6, we report the leakage ratio between the two leakage analysis corners with the original standard cell netlist and with our new netlist. All data are presented with the an input slew of 180 ps and output load of 4.7 ff. We see an average of 11% decrease for the variabilities of delay. As we performed our litho simulation across process window, through exposure dose and depth of focus rather than at a normal process condition, we think that is a significant source of the variability. However, we strongly believe that litho simulation through process window is absolutely necessary in order to capture lithography effect properly in process corner-based design flow. The leakage analysis shows that the new netlist of the standard cells have far less variability for leakage, with the average ratio less than half of that of the original netlist. We would also want to point out that because transistor leakage is exponential to the transistor gate length, doing leakage calculation with this methodology can help identify lithography-sensitive design patterns for leakage and thus help improve standard cell design robustness in terms of leakage variability. With the improvement of OPC and SRAF generation from the foundry, we believe we will see better design variability control for both timing and leakage.

### 3.2 Design implementation

We apply our newly characterised standard cell library to one of the low-power, high-speed hard macros of our 65 nm designs for timing analysis. We use our standard timing signoff flow for this analysis, with the same timing constraints as the original design.

Fig. 11 shows the timing variability reduction for the 400 most timing critical paths in the design. Timing variability for a path is defined as the path delay difference between the best and worst timing corners. Use our methodology, we are able to reduce the variability on an average of about 330 ps. With the average path delay variability at 3 ns, we reduce the variability by 11%, which is consistent with our standard cell analysis.

We present data for leakage analysis for several 65 nm hard macros in Table 2. Columns 3 and 4 are the leakage ratio between the two leakage analysis corners for original and new netlists for each block. The data are once again very consistent with cell-level analysis.

![Fig. 11](image1.png) **Timing variability reduction for critical paths**

![Fig. 12](image2.png)

**Fig. 12** Delay path timing changes

a Delay change of setup paths
b Delay change of hold paths

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**Table 2: Leakage variability analysis**

<table>
<thead>
<tr>
<th>Block</th>
<th>Instance count</th>
<th>Original leakage ratio</th>
<th>New leakage ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>block 1</td>
<td>87 265</td>
<td>14.4</td>
<td>6.7</td>
</tr>
<tr>
<td>block 2</td>
<td>20 582</td>
<td>15.0</td>
<td>6.5</td>
</tr>
<tr>
<td>block 3</td>
<td>38 515</td>
<td>19.8</td>
<td>8.8</td>
</tr>
<tr>
<td>block 4</td>
<td>94 165</td>
<td>19.3</td>
<td>8.3</td>
</tr>
<tr>
<td>block 5</td>
<td>236 832</td>
<td>18.5</td>
<td>8.0</td>
</tr>
<tr>
<td>ave</td>
<td>95 471.8</td>
<td>17.4</td>
<td>7.7</td>
</tr>
</tbody>
</table>
3.3 BEOL comparison

We use a 65 nm high-speed IP block implemented with standard cells as our test case. There are about 2k placed standard cell instances in this test case. As described in previous section, we performed two STA simulations based on different approaches for lithography effects on interconnection, one with routing metal drawn shape and the other with litho contour converted polygon for routing metals. We generated STA reports for all endpoints of the design for both setup and hold delays. We then compare the difference of the delays with the two STA results for each endpoint. The difference is shown in Figs. 12a and 12b.

The experiment shows that the timing impact for metal litho effects is within 1%–2% for both setup and hold delay paths except one hold delay path, which is about 3.6%. Additionally, litho effects cause some paths to have larger delays, other paths to have smaller delays. In fact, the small differences caused by litho effects on routing metals are in the same order of the errors in STA flow and the parasitic extraction.

4 Conclusion

In this paper, we proposed a new lithography-aware design methodology. The systematic lithography effects are considered in the design flow to reduce design pessimism. For polysilicon transistor gates, we introduced dummy poly into the standard cell to achieve context independency of the standard cell timing model; for interconnection, we verified that traditional lookup table-based methodology is still applicable considering lithography effect. Our methodology can be easily incorporated into current design flow with virtually no impact on design schedule. We performed a lithography simulation with foundry validated and calibrated production lithography models across process window, and extracted the electrical parameters from the lithography images and applied STA on the design. As a result, we have reduced the pessimism introduced by the traditional process corners methodology for timing and leakage analysis for real 65 nm designs.

5 References