DC & Transient Responses

DC Response

- DC Response: $V_{\text{out}}$ vs. $V_{\text{in}}$ for a gate
- Ex: Inverter
  - When $V_{\text{in}} = 0 \rightarrow V_{\text{out}} = V_{\text{DD}}$
  - When $V_{\text{in}} = V_{\text{DD}} \rightarrow V_{\text{out}} = 0$
  - In between, $V_{\text{out}}$ depends on transistor size and current
  - By KCL, must settle such that $I_{\text{dsn}} = |I_{\text{dsp}}|$
  - We could solve equations
  - But graphical solution gives more insight

\[\begin{array}{c}
V_{\text{dd}} \\
\downarrow \\
V_{\text{in}} \\
\downarrow \\
\downarrow \quad I_{\text{dsn}} \\
\downarrow \\
\downarrow \\
I_{\text{dsp}} \\
\downarrow \\
V_{\text{out}} \\
\end{array}\]
Transistor Operation

- Current depends on region of transistor behavior
- For what $V_{in}$ and $V_{out}$ are nMOS and pMOS in
  - Cutoff?
  - Linear?
  - Saturation?

nMOS Operation

<table>
<thead>
<tr>
<th>Cutoff</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gsn} &lt;$</td>
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</tr>
<tr>
<td>$V_{dsn} &lt;$</td>
<td>$V_{dsn} &gt;$</td>
<td></td>
</tr>
</tbody>
</table>

![nMOS Circuit Diagram](image)
### nMOS Operation

#### Cutoff
- $V_{gsn} < V_{tn}$
- $V_{dsn} < V_{gsn} - V_{tn}$

#### Linear
- $V_{gsn} > V_{tn}$
- $V_{dsn} < V_{gsn} - V_{tn}$

#### Saturated
- $V_{gsn} > V_{tn}$
- $V_{dsn} > V_{gsn} - V_{tn}$

![nMOS Circuit Diagram](image)

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### nMOS Operation

#### Cutoff
- $V_{gsn} < V_{tn}$
- $V_{dsn} < V_{gsn} - V_{tn}$

#### Linear
- $V_{gsn} > V_{tn}$
- $V_{dsn} < V_{gsn} - V_{tn}$

#### Saturated
- $V_{gsn} > V_{tn}$
- $V_{dsn} > V_{gsn} - V_{tn}$

![nMOS Circuit Diagram](image)
nMOS Operation

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<tr>
<td>$V_{gsn} &lt; V_{tn}$</td>
<td>$V_{gsn} &gt; V_{in}$</td>
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</tr>
<tr>
<td>$V_{in} &lt; V_{tn}$</td>
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</tr>
<tr>
<td>$V_{dsn} &lt; V_{gsn} - V_{tn}$</td>
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<tr>
<td>$V_{out} &lt; V_{in} - V_{tn}$</td>
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$pMOS$ Operation

<table>
<thead>
<tr>
<th>Cutoff</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gsp} &gt;$</td>
<td>$V_{gsp} &lt;$</td>
<td>$V_{gsp} &lt;$</td>
</tr>
<tr>
<td>$V_{dsp} &gt;$</td>
<td>$V_{dsp} &lt;$</td>
<td>$V_{dsp} &lt;$</td>
</tr>
</tbody>
</table>
### pMOS Operation

<table>
<thead>
<tr>
<th>Cutoff</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gsp} &gt; V_{tp}$</td>
<td>$V_{gsp} &lt; V_{tp}$</td>
<td>$V_{gsp} &lt; V_{tp}$</td>
</tr>
<tr>
<td></td>
<td>$V_{dsp} &gt; V_{gsp} - V_{tp}$</td>
<td>$V_{dsp} &lt; V_{gsp} - V_{tp}$</td>
</tr>
</tbody>
</table>

- $V_{gsp}$: Gate-source voltage
- $V_{tp}$: Threshold voltage
- $V_{dsp}$: Drain-source voltage
- $V_{in}$: Input voltage
- $V_{out}$: Output voltage
- $V_{DD}$: Power supply voltage

### pMOS Operation

<table>
<thead>
<tr>
<th>Cutoff</th>
<th>Linear</th>
<th>Saturated</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{gsp} &gt; V_{tp}$</td>
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<td>$V_{dsp} &lt; V_{gsp} - V_{tp}$</td>
</tr>
</tbody>
</table>

\[
V_{gsp} = V_{in} - V_{DD} \quad V_{tp} < 0 \\
V_{dsp} = V_{out} - V_{DD}
\]
pMOS Operation

Cutoff | Linear | Saturated
---|---|---
$V_{gsp} > V_{tp}$ | $V_{gsp} < V_{tp}$ | $V_{gsp} < V_{tp}$
$V_{in} > V_{DD} + V_{tp}$ | $V_{in} < V_{DD} + V_{tp}$ | $V_{in} < V_{DD} + V_{tp}$

$V_{dsp} > V_{gsp} - V_{tp}$ | $V_{dsp} > V_{gsp} - V_{tp}$ | $V_{dsp} > V_{gsp} - V_{tp}$
$V_{out} > V_{in} - V_{tp}$ | $V_{out} > V_{in} - V_{tp}$ | $V_{out} > V_{in} - V_{tp}$

$V_{gsp} = V_{in} - V_{DD}$
$V_{dsp} = V_{out} - V_{DD}$

V_{in} \quad \rightarrow \quad I_{dsn} \quad \downarrow \quad V_{out}

I-V Characteristics

- Make pMOS is wider than nMOS such that $\beta_n = \beta_p$
Current vs. $V_{out}$, $V_{in}$

<table>
<thead>
<tr>
<th>$V_{in0}$</th>
<th>$V_{in5}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{in1}$</td>
<td>$V_{in4}$</td>
</tr>
<tr>
<td>$V_{in2}$</td>
<td>$V_{in3}$</td>
</tr>
<tr>
<td>$V_{in3}$</td>
<td>$V_{in2}$</td>
</tr>
<tr>
<td>$V_{in4}$</td>
<td>$V_{in1}$</td>
</tr>
</tbody>
</table>

For a given $V_{in}$:
- Plot $I_{dsn}$, $I_{dsp}$ vs. $V_{out}$
- $V_{out}$ must be where $|currents|$ are equal in

Load Line Analysis
Load Line Analysis

- $V_{in} = 0$

\[ V_{in0}, I_{dsn}, |I_{dspl}| \rightarrow V_{out} \rightarrow V_{DD} \]

Load Line Analysis

- $V_{in} = 0.2V_{DD}$

\[ I_{dsn}, |I_{dspl}| \rightarrow V_{in1} \rightarrow V_{out} \rightarrow V_{DD} \]
Load Line Analysis

- $V_{in} = 0.4V_{DD}$

- $V_{in} = 0.6V_{DD}$
Load Line Analysis

- $V_{in} = 0.8V_{DD}$

![Graph showing load line analysis with $V_{in} = 0.8V_{DD}$]

Load Line Analysis

- $V_{in} = V_{DD}$

![Graph showing load line analysis with $V_{in} = V_{DD}$]
Load Line Summary

DC Transfer Curve

Transcribe points onto $V_{in}$ vs. $V_{out}$ plot
## Operating Regions

- **Revisit transistor operating regions**

**Table:**

<table>
<thead>
<tr>
<th>Region</th>
<th>nMOS</th>
<th>pMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Cutoff</td>
<td>Linear</td>
</tr>
<tr>
<td>B</td>
<td>Saturation</td>
<td>Linear</td>
</tr>
<tr>
<td>C</td>
<td>Saturation</td>
<td>Saturation</td>
</tr>
<tr>
<td>D</td>
<td>Linear</td>
<td>Saturation</td>
</tr>
<tr>
<td>E</td>
<td>Linear</td>
<td>Cutoff</td>
</tr>
</tbody>
</table>

**Diagram:**

- A: Cutoff
- B: Linear
- C: Saturation
- D: Saturation
- E: Cutoff

**Graph:**

- V_in
- V_out
Beta Ratio

- If $\beta_p / \beta_n \neq 1$, switching point will move from $V_{DD}/2$
- Called *skewed gate*
- Other gates: collapse into equivalent inverter

Noise Margins

- How much noise can a gate input see before it does not recognize the input?
To maximize noise margins, select logic levels at $V_{DD}$ and $V_{IN}$. The output level, $V_{OUT}$, should be such that $\beta_p/\beta_n > 1$.

To maximize noise margins, select logic levels at the unity gain point of the DC transfer characteristic. This point is defined by the slope of unity gain, which is $-1$. The output level, $V_{OUT}$, should be such that $\beta_p/\beta_n > 1$.
Pass Transistors

- We have assumed source is grounded
- What if source > 0?
  - e.g. pass transistor passing $V_{DD}$
- $V_g = V_{DD}$
  - If $V_s > V_{DD} - V_t$, $V_{gs} < V_t$
  - Hence transistor would turn itself off
- nMOS pass transistors pull no higher than $V_{DD} - V_{th}$
  - Called a degraded “1”
  - Approach degraded value slowly (low $I_{ds}$)
- pMOS pass transistors pull no lower than $|V_{tp}|$
Pass Transistor Ckts

\[ V_s = V_{DD} - V_{tn} \]

\[ V_s = |V_{tp}| \]

\[ V_{DD} \]

\[ V_{SS} \]
Transient Response

- DC analysis tells us $V_{out}$ if $V_{in}$ is constant
- Transient analysis tells us $V_{out}(t)$ if $V_{in}(t)$ changes
  - Requires solving differential equations
- Input is usually considered to be a step or ramp
  - From 0 to $V_{DD}$ or vice versa

Inverter Step Response

- Ex: find step response of inverter driving load cap

$V_{in}(t) =$

$V_{out}(t < t_0) =$

$\frac{dV_{out}(t)}{dt} =$
Inverter Step Response

- Ex: find step response of inverter driving load cap

\[ V_{in}(t) = u(t-t_0)V_{DD} \]
\[ V_{out}(t < t_0) = V_{DD} \]
\[ \frac{dV_{out}(t)}{dt} = \]

![Inverter Circuit Diagram]
Ex: find step response of inverter driving load cap

\[ V_{in}(t) = u(t - t_0)V_{DD} \]

\[ V_{out}(t < t_0) = V_{DD} \]

\[ \frac{dV_{out}(t)}{dt} = -\frac{I_{dsn}(t)}{C_{load}} \]

\[ I_{dsn}(t) = \begin{cases} 
0 & t \leq t_0 \\
\frac{\beta}{2}(V_{dd} - V) & V_{out} > V_{dd} - V \\
\beta \left(V_{dd} - V - \frac{V_{out}(t)}{2}\right) & V_{out} < V_{dd} - V
\end{cases} \]
Inverter Step Response

- Ex: find step response of inverter driving load cap

\[
V_{in}(t) = u(t - t_0)V_{DD}
\]

\[
V_{out}(t < t_0) = V_{DD}
\]

\[
\frac{dV_{out}(t)}{dt} = \frac{-I_{dsn}(t)}{C_{load}}
\]

\[
I_{dsn}(t) = \begin{cases} 
0 & t \leq t_0 \\
\frac{2}{\pi}(V_{dd} - V) & V_{out} > V_{dd} - V_i \\
\beta\left(V_{dd} - V_i - \frac{V_{out}(t)}{2}\right)V_{out}(t) & V_{out} < V_{dd} - V_i 
\end{cases}
\]

Delay Definitions

- \( t_{pdr} \): rising propagation delay
  - From input to rising output crossing \( V_{DD}/2 \)
- \( t_{pdl} \): falling propagation delay
  - From input to falling output crossing \( V_{DD}/2 \)
- \( t_{pd} \): average propagation delay
  - \( t_{pd} = (t_{pdr} + t_{pdl})/2 \)
- \( t_r \): rise time
  - From output crossing \( 0.1 \ V_{DD} \) to \( 0.9 \ V_{DD} \)
- \( t_f \): fall time
  - From output crossing \( 0.9 \ V_{DD} \) to \( 0.1 \ V_{DD} \)
Simulated Inverter Delay

- Solving differential equations by hand is too hard
- SPICE simulator solves the equations numerically
  - Uses more accurate I-V models too!
- But simulations take time to write

Inverter Fall Time

\[
I_{dsn}(t) = \begin{cases} 
0 & t \leq t_0 \\
\frac{g}{2}(V_{in} - V_i)^2 & V_{in} > V_{DD} - V_i \\
\beta \left(V_{DD} - V_i - \frac{V_{in}(t)}{2}\right) & V_{in} < V_{DD} - V_i 
\end{cases}
\]

- \( t_1: 0.9V_{DD} = \Rightarrow (V_{DD} - V_i) \)
- \( t_2: (V_{DD} - V_i) = \Rightarrow 0.1V_{DD} \)
**Fall Time: Saturation Region**

\[
C_{\text{load}} \frac{dV_{\text{out}}}{dt} + \frac{\beta}{2} (V_{\text{DD}} - V_t)^2 = 0
\]

\[
t_f = 2 \frac{C_{\text{load}}}{\beta (V_{\text{DD}} - V_t)^2} \int_{V_{\text{DD}} - V_t}^{0.9V_{\text{DD}}/2} dV_{\text{out}} = 2C_{\text{load}}(V_t - 0.1V_{\text{DD}}) \frac{V_{\text{DD}} - V_t}{\beta (V_{\text{DD}} - V_t)^2}
\]

**Fall Time: Linear Region**

\[
t_f = \frac{C_{\text{load}}}{\beta (V_{\text{DD}} - V_t)^2} \int_{0.1V_{\text{DD}}}^{V_{\text{DD}} - V_t} \frac{dV_{\text{out}}}{V_{\text{out}}^2} = \frac{V_{\text{DD}} - V_t}{2(V_{\text{DD}} - V_t)} - V_{\text{out}}
\]

\[
t_f = \frac{C_{\text{load}}}{\beta V_{\text{DD}}(1 - \frac{V_t}{V_{\text{DD}}})} \ln(19 - 20 \frac{V_t}{V_{\text{DD}}})
\]
Overall Fall Time

\[ t_f = \frac{2C_{load}}{\beta V_{DD}(1-n)} \left[ \frac{n-0.1}{1-n} + \frac{1}{2} \ln(19-20n) \right] \]

\[ \approx k \times \frac{C_{load}}{\beta V_{DD}} \]

\[ n = V_f/V_{DD} \]

Rise/Fall Time and Delay

- Approximately
  - \( t_{dr} = t_r/2 \)
  - \( t_{df} = t_r/2 \)