Combinational Circuits

Example 1

module mux(input s, d0, d1, output y);
    assign y = s ? d1 : d0;
endmodule

1) Sketch a design using AND, OR, and NOT gates.
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Example 2

2) Sketch a design using NAND, NOR, and NOT gates. Assume ~S is available.
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![DIAGRAM]

Bubble Pushing

- Start with network of AND / OR gates
- Convert to NAND / NOR + inverters
- Push bubbles around to simplify logic
  - Remember DeMorgan’s Law

![DIAGRAM]
Compound Gates

- Logical Effort of compound gates

<table>
<thead>
<tr>
<th></th>
<th>AOI121</th>
<th>AOI22</th>
<th>Complex AOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>unit inverter</td>
<td>$Y = \overline{A}$</td>
<td>$Y = \overline{A}.B + C$</td>
<td>$Y = \overline{A}.B + C \cdot \overline{D}$</td>
</tr>
<tr>
<td>$A$</td>
<td>$B$</td>
<td>$C$</td>
<td>$D$</td>
</tr>
<tr>
<td>$Y = \overline{A}$</td>
<td>$A$</td>
<td>$B$</td>
<td>$C$</td>
</tr>
<tr>
<td>$g_A = 3/3$</td>
<td>$g_B = 6/3$</td>
<td>$g_C = 6/3$</td>
<td>$g_D = 6/3$</td>
</tr>
<tr>
<td>$p = 3/3$</td>
<td>$g_A = 5/3$</td>
<td>$g_B = 6/3$</td>
<td>$g_D = 6/3$</td>
</tr>
<tr>
<td>$g_C = 5/3$</td>
<td>$p = 7/3$</td>
<td></td>
<td>$p = 12/3$</td>
</tr>
</tbody>
</table>

ECEN 454
Our parasitic delay model was too simple
- Calculate parasitic delay for $Y$ falling
  - If $A$ arrives latest?
  - If $B$ arrives latest?

\[ \begin{align*}
A & \xrightarrow{2} 2 \xrightarrow{2} 6C \\
B & \xrightarrow{2} \times \xrightarrow{2} 2C \\
& \xrightarrow{X} Y
\end{align*} \]
**Inner & Outer Inputs**

- *Outer* input is closest to rail (B)
- *Inner* input is closest to output (A)

*If input arrival time is known*
- Connect latest input to inner terminal

**Beyond Static CMOS**

- What makes a circuit fast?
  - \( I = C \frac{dV}{dt} \rightarrow t_{pd} \propto (C/I) \Delta V \)
  - low capacitance
  - high current
  - small swing

- Logical effort is proportional to \( C/I \)

- pMOS are the enemy!
  - High capacitance for a given current

- Can we take the pMOS capacitance off the input?

- Various circuit families try to do this…
Pseudo-nMOS

- In the old days, nMOS processes had no pMOS
  - Instead, use pull-up transistor that is always ON

- In CMOS, use a pMOS that is always ON
  - Ratio issue
  - Make pMOS about ¼ effective strength of pulldown network

Pseudo-nMOS Power

- Pseudo-nMOS draws power whenever Y = 0
  - Called static power  \( P = I \cdot V_{DD} \)
  - A few mA / gate * 1M gates would be a problem
  - This is why nMOS went extinct!

- Use pseudo-nMOS sparingly for wide NORs

- Turn off pMOS when not in use