

Fall 2009 Department of Electrical and Computer Engineering

## **ECEN 454 Digital Integrated Circuit Design**

### **Instructor**

Prof. Peng Li  
Office: 333M WERC  
Phone: 845-1612 Email: pli@tamu.edu  
URL: <http://www.ece.tamu.edu/~pli>  
Office hours: M/W: 10:30am – 11:20am or by appointments

### **TA**

Srinath Narasimhan, Email: [srinathn@neo.tamu.edu](mailto:srinathn@neo.tamu.edu)

### **Lectures**

M/W: 9:10am – 10:00am ZACH 223A  
**Class website:** <http://dropzone.tamu.edu/~pli/454Fall09/>

### **Lab**

Section I: F 9:00am-11:00am ZACH 213A  
Section II: W 6:30 pm - 8:30 pm ZACH 213A  
Section III: F 11:20 am - 1:20 pm ZACH 213A  
Lab webpage: <http://people.tamu.edu/~srinathn/ecen454.html>

### **Text**

**CMOS VLSI Design: A Circuits and Systems Perspective**, 3rd Edition, by Neil Weste and David Harris, Addison Wesley, 2005.

### **References**

Digital Integrated Circuits, A Design Perspective, by Rabaey, et al. Prentice Hall.  
CMOS Digital Integrated Circuits – Analysis and Design, By Kang and Leblebici, Third Edition, McGraw Hill.

### **Prerequisites**

ELEN248 (Introduction to Digital Systems Design) or equivalents

### **Course Overview**

This course provides a comprehensive introduction to various aspects of modern digital integrated circuit design, including IC fabrication processes, MOS transistor device characteristics, schematic and layout design, combinational and sequential logic, interconnect, datapaths, memories, timing, and clock distribution. Various logic families and design styles are introduced. In lab sessions, students will gain hands-on design experience through the use of the state-of-art commercial design tools.

## Lecture Agenda (tentative)

1. Introduction
2. CMOS circuit overview
3. Fabrication and layout
4. MOS transistor IV characteristics and parasitics
5. DC and transient characteristics
6. Delay and power Estimation
7. Logic effort and gate sizing
8. Interconnect
9. SPICE simulation
10. Combinational circuits
11. Sequential circuits
12. Clock distribution
13. Datapath functional units
14. Semiconductor memories
15. Advanced design considerations

## Grading

<b>Homework</b>	5%
<b>Mid-term</b>	20%
<b>Final Exam</b>	25%
<b>Labs</b>	50%

Late homework: 20% penalty/day.

Check the lab webpage for lab grading policy.

## Lab Safety Agreement

The forms will be distributed and they should be reviewed, filled out, and turned back into the department.

## Logistics

Check the class website for important logistical issues.