MOS Transistor I-V Characteristics and Parasitics

Facts about Transistors

- So far, we have treated transistors as ideal switches
- An ON transistor passes a finite amount of current
  - Depends on terminal voltages
  - Derive current-voltage (I-V) relationships
- Transistor gate, source, drain all have capacitances
  - \( I = C \left( \frac{\Delta V}{\Delta t} \right) \rightarrow \Delta t = \frac{C}{I} \Delta V \)
  - Capacitance and current determine speed
- Also explore what a “degraded level” really means
MOS Capacitor

- Gate and body form a MOS capacitor
- Operating modes:
  - Accumulation
  - Depletion
  - Inversion

![Diagram of MOS Capacitor Modes]

Terminal Voltages for NMOS

- Mode of operation depends on \( V_g, V_d, V_s \)
  - \( V_{gs} = V_g - V_s \)
  - \( V_{gd} = V_g - V_d \)
  - \( V_{ds} = V_d - V_s = V_{gs} - V_{gd} \)
- Source and drain are symmetric diffusion terminals
  - By convention, source is the terminal at a lower voltage
  - Hence \( V_{ds} \geq 0 \)
- nMOS body is grounded.
- Three regions of operation
  - **Cutoff**
  - **Linear**
  - **Saturation**
nMOS Cutoff

- No channel
- \( I_{ds} = 0 \)

nMOS Linear

- Channel forms
- Current flows from d to s
  - \( \text{e}^+ \) from s to d
- \( I_{ds} \) increases with \( V_{ds} \)
- Similar to a linear resistor
nMOS Saturation

- Channel pinches off
- \( I_{ds} \) independent of \( V_{ds} \) (approximately)
- We say the drain current saturates
- Similar to a voltage controlled current source

\[ V_{gs} > V_t \]
\[ V_{gd} < V_t \]
\[ V_{ds} > V_{gs} - V_t \]

I-V Characteristics

- In Linear region, \( I_{ds} \) depends on
  - How much charge is in the channel?
  - How fast is the charge moving?
Channel Charge

- MOS structure looks like parallel plate capacitor while operating in inversion
  - Gate – oxide – channel
- \(Q_{\text{channel}} = CV\)
- \(C = \)
MOS structure looks like parallel plate capacitor while operating in inversion
- Gate – oxide – channel
- \( Q_{\text{channel}} = CV \)
- \( C = C_g = \varepsilon_{\text{ox}} \frac{W}{t_{\text{ox}}} = C_{\text{ox}} W \)
- \( V = V_{g} - V_t = (V_{gs} - V_{ds}/2) - V_t \)

\[ C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \]
Carrier velocity

- Charge is carried by e-
- Carrier velocity \( v \) proportional to lateral E-field between source and drain
  \[ v = \mu E \]

\( \mu \) called mobility
Carrier velocity

- Charge is carried by e-
- Carrier velocity $v$ proportional to lateral E-field between source and drain
  - $v = \mu E$
  - $E = \frac{V_{ds}}{L}$
  - $\mu$ called mobility
- Time for carrier to cross channel:
  - $t = \frac{L}{v}$
Now we know
- How much charge $Q_{\text{channel}}$ is in the channel
- How much time $t$ each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$
nMOS Linear I-V

- Now we know
  - How much charge $Q_{\text{channel}}$ is in the channel
  - How much time $t$ each carrier takes to cross

$$I_{ds} = \frac{Q_{\text{channel}}}{t}$$

$$= \mu C_{ox} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds}$$

$$= \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} \quad \beta = \mu C_{ox} \frac{W}{L}$$

nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
- When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} =$$
nMOS Saturation I-V

- If $V_{gd} < V_t$, channel pinches off near drain
  - When $V_{ds} > V_{dsat} = V_{gs} - V_t$
- Now drain voltage no longer increases current

$$I_{ds} = \beta \left( V_{gs} - V_t - \frac{V_{dsat}}{2} \right) V_{dsat}$$

$$= \frac{\beta}{2} (V_{gs} - V_t)^2$$
nMOS I-V Summary

- **Shockley 1st order transistor models**

\[ I_{ds} = \begin{cases} 
0 & V_{gs} < V_t \quad \text{cutoff} \\
\beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\
\frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} 
\end{cases} \]

**Example**

- For a 0.6 \( \mu m \) process
  - \( t_{ox} = 100 \) Å
  - \( \mu = 350 \) cm\(^2\)/V*s
  - \( V_t = 0.7 \) V
- Plot \( I_{ds} \) vs. \( V_{ds} \)
  - \( V_{gs} = 0, 1, 2, 3, 4, 5 \)
  - Use \( W/L = 4/2 \lambda \)

\[ \beta = \mu C_W \frac{W}{L} = (350) \left( \frac{3.9 \times 8.85 \times 10^{-3}}{100 \times 10^{-6}} \right) \left( \frac{W}{L} \right) = 120 \frac{W}{L} \mu A/V^2 \]
pMOS I-V

- All dopings and voltages are inverted for pMOS
  - Source is the more positive terminal
- Mobility \( \mu_p \) is determined by holes
  - Typically 2-3x lower than that of electrons \( \mu_n \)
  - 120 cm²/V·s in AMI 0.6 μm process
- Thus pMOS must be wider to provide same current
  - In this class, assume \( \mu_n / \mu_p = 2 \)

Non-ideal I-V Effects

- Velocity saturation
  - Due to lateral E-field
- Mobility degradation
  - Due to vertical E-field
- Channel length modulation
- Leakage current
- Body effect
- Temperature dependence
- And many more...
Channel Length Modulation

- Ideally, $I_{ds}$ is independent of $V_{ds}$ in saturation
- Reverse-biased p-n junction between drain and body forms a depletion region with width $L_d$
- $L_{\text{EFF}} = L - L_d$
- $L_d$ increases with $V_{db}$ or $V_{ds}$
- $I_{ds}$ increases slightly with $V_{ds}$

Velocity Saturation

- Ideally, carrier drift velocity increases linearly with lateral field ($V_{ds}/L$)
- If lateral field is very strong, the velocity saturated due to scattering
- $\alpha$-power law model
- As velocity saturated, increasing $V_{gs}$ has less effect
- As velocity saturated, no benefit to raise $V_{DD}$
Velocity Saturation

- Velocity saturation
- Impact of the lateral electrical field

\[ \nu_n (\text{m/s}) \]

\[ \xi_c = 1.5 \]

\[ \xi (\text{V/\mu m}) \]

\[ \nu_{sat} = 10^5 \]

Constant velocity

Constant mobility (slope = \( \mu \))

Velocity Saturation

- Velocity saturation

Long-channel device

Short-channel device

\[ V_{GS} = V_{DD} \]

\[ V_{DSAT} \]

\[ V_{GS} - V_T \]

\[ V_{DS} \]

Not \( V_{GS} - V_T \) !!!
Mobility Degradation

- Strong vertical field ($V_{gs}$) causes scattering, reduces carrier mobility
- Captured in $\alpha$-power law model
  - By $\alpha$

Short-Channel Effects (5)

- Mobility degradation
  - Impact of vertical electric field

![Graph showing mobility degradation](image)
Leakage Current

- **Subthreshold leakage**
  \[ I_{ds} = I_{ds0} \cdot e^{\frac{V_{gs} - V_t}{mV_T}} \left( 1 - e^{\frac{-V_{ds}}{V_T}} \right) \]
  - Thermal voltage: \( V_T = kT/q \) (@300K ~26mv) \( k \): Boltzmann’s constant

- **Junction leakage**

- **Gate tunneling**

Body Effect

- **\( V_{sb} \) affects threshold voltage**
  \[ V_t = V_{th} + \gamma(\sqrt{2\phi_F} + V_{bs} - \sqrt{2\phi_F}) \]
  - \( \phi_F \): Fermi potential (in bulk)

- **Body voltage affects both speed and leakage**
  - Forward body bias (FBB)
  - Reverse body bias (RBB)
# Temperature Dependence

- When temperature increases
  - Carrier mobility decreases, ON current decreases
  - Threshold voltage decreases, leakage increases

# Capacitance

- Any two conductors separated by an insulator have capacitance

- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation

- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion
**Gate Capacitance**

- Approximate channel as connected to source
- \( C_{gs} = \varepsilon_{ox}WL/t_ox = C_{ox}WL = C_{permicron}W \)
- \( C_{permicron} \) is typically about 2 fF/\( \mu \)m

**Diffusion Capacitance**

- \( C_{sb}, C_{db} \)
- Undesirable, called *parasitic* capacitance
- Capacitance depends on area and perimeter
  - Use small diffusion nodes
  - Comparable to \( C_g \) for contacted diff
  - \( \frac{1}{2} C_g \) for uncontacted
  - Varies with process
Diffusion Capacitance

- We assumed contacted diffusion on every s/d.
- Good layout minimizes diffusion area
- Ex: NAND3 layout shares one diffusion contact
  - Reduces output capacitance by 2C
  - Merged uncontacted diffusion might help too

Activity

1) If the width of a transistor increases, the current will
   increase decrease not change
2) If the length of a transistor increases, the current will
   increase decrease not change
3) If the supply voltage of a chip increases, the maximum
   transistor current will
   increase decrease not change
4) If the width of a transistor increases, its gate capacitance will
   increase decrease not change
5) If the length of a transistor increases, its gate capacitance will
   increase decrease not change
6) If the supply voltage of a chip increases, the gate capacitance
   of each transistor will
   increase decrease not change
Activity

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