Instructor
Prof. Peng Li
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Lectures
MWF 11:30-12:20pm, 223D Zachry

Office hours
MW 3:30-4:30pm or by appointment

Teaching Assistant
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Course Website
http://dropzone.tamu.edu/~pli/468Fall08

Lab Website
http://people.tamu.edu/~akshitdayal/468/468fall2008.html

Course Description
The main focus of the course is on Verilog hardware description language (HDL) and its applications in VLSI logic design, simulation and verification. The lab sessions will provide students the opportunity to learn modern ASIC design methodologies, flows and design tools.

Textbook

Prerequisite
ELEN 248 Introduction to Digital System Design or equivalent

Grading
Homework 10%, Midterm1 20%, Midterm2 20%, Labs 50%
Late homework: 25% penalty per extra day; see the Lab website for detailed Lab grading policies.

Lecture Topics (tentative)
1. Introduction (Ch. 1)
2. Hardware Modeling (Ch. 2)
3. Simulation and testbench (Ch. 3)
4. Data types and operators (Ch. 4)
5. User-defined primitives (Ch. 5)
6. Delay models (Ch. 6)
7. System tasks, functions, syntax and behavioral modeling 1 (App. E, F, H, Ch. 7)
8. Behavioral modeling 2 (Ch. 7)
9. Behavioral modeling 3 (Ch. 7)
10. Behavioral modeling 4 (Ch. 7)
11. Switch-level models (Ch. 11)
12. Synthesis of combinational logic 1(Ch. 8)
13. Synthesis of combinational logic 2 (Ch. 8)
14. Synthesis of sequential logic (Ch. 9)
15. Synthesis of language constructs 1 (Ch. 10)
16. Synthesis of language constructs 2 (Ch. 10)
17. MIPS processor
18. VHDL
19. FPGA (Ch. 13), A tutorial by Brown and Rose
20. HDL coding styles
21. Timing verification
22. Testing
23. Design for testability
24. Built-in self-test
25. Interconnect timing optimization
26. Gate and interconnect optimization
27. Logic and placement synthesis
28. Low power design

**Logistics**

Check the course website for important logistical issues.