

Impact of Photolithography and Mask Variability on Interconnect Parasitics *

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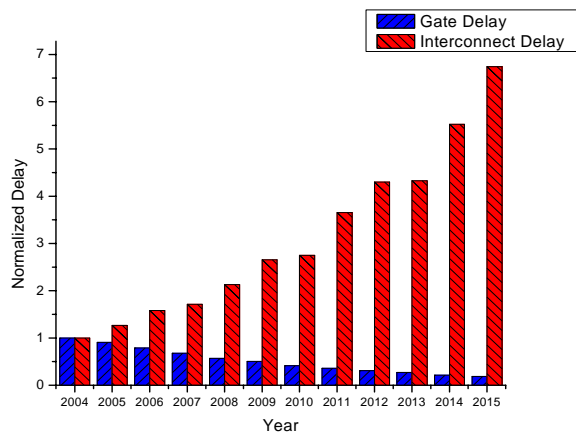
ABSTRACT

Due to photolithography effects and manufacture process variations, the actual features printed on wafer are different from the designed ones. This difference results in the inaccuracy on parasitic extraction, which is critical for timing verification and design for manufacturability. Most of the current layout parasitic extraction (LPE) tools ignore these effects and can cause as high as 20% errors. This paper proposes a new strategy to extract interconnect parasitics with the consideration of photolithography effects and process variations. Based on the feedback from lithography simulation, a shape correction process is setup to adjust the interconnect structure for LPE tools. Compared with the traditional extraction methodology, the parasitics extracted from this adjusted geometry are more accurate. This method can be implanted into the current design flow with minimum change. Meanwhile, this paper studies the impacts of mask critical dimension (CD) variations on interconnect parasitics. The variability analysis is based on PROLITH^① lithography simulation software and is tested on RAPHAEL^{TM②} interconnect library. The results show a high nonlinear relationship between the mask variation and the interconnect parasitics.

Keyword: Parasitic Extraction, DFM, Lithography Simulation, Mask Variability

1. INTRODUCTION

As the increasing speed of the circuit and the shrinking feature sizes of semiconductor devices, interconnect variation



results in more stringent requirements for the circuit designers. A key issue is to understand the sources of the variations and what are their impacts on circuit performance. In [1], a process model for sensitivity to different variations is derived for a clock tree. In [2], a methodology is proposed for the modeling of effects of systematic intra-die variations on circuit performance. In [3], an integrated variation analysis technique is proposed to consider both the effects of systematic and random variations simultaneously. All these studies require very accurate parasitic extraction and performance analysis. Therefore, extracting the interconnect parasitics (RLC) efficiently and accurately becomes more important for circuit design and analysis as the feature size shrinking. Figure 1 shows the normalized interconnect and gate delay (assuming the delay in 2004 is 1) in the coming decade projected by the International technology road of semiconductor (ITRS) [4]. This figure clearly shows that

^① PROLOTH is a lithography process simulation tool from KLA-Tencor Corporation.

^② RAPHAELTM is an interconnect analysis software product from Synopsys, Inc.

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the interconnect delay will become a more important issue in the next decade. Meanwhile, due to sub-wavelength lithography effects and process variations (such as mask size, etching speed, exposure dose and focal position variations, etc.), the features appeared on layouts are different from that printed on wafers. Therefore, considering these variations, the traditional LPE methods need to be improved to handle nanoscale interconnect structures.

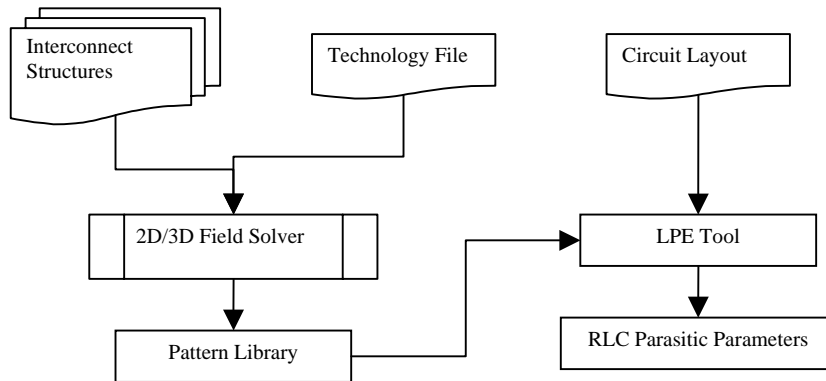


Figure 2. Traditional LPE Methodology

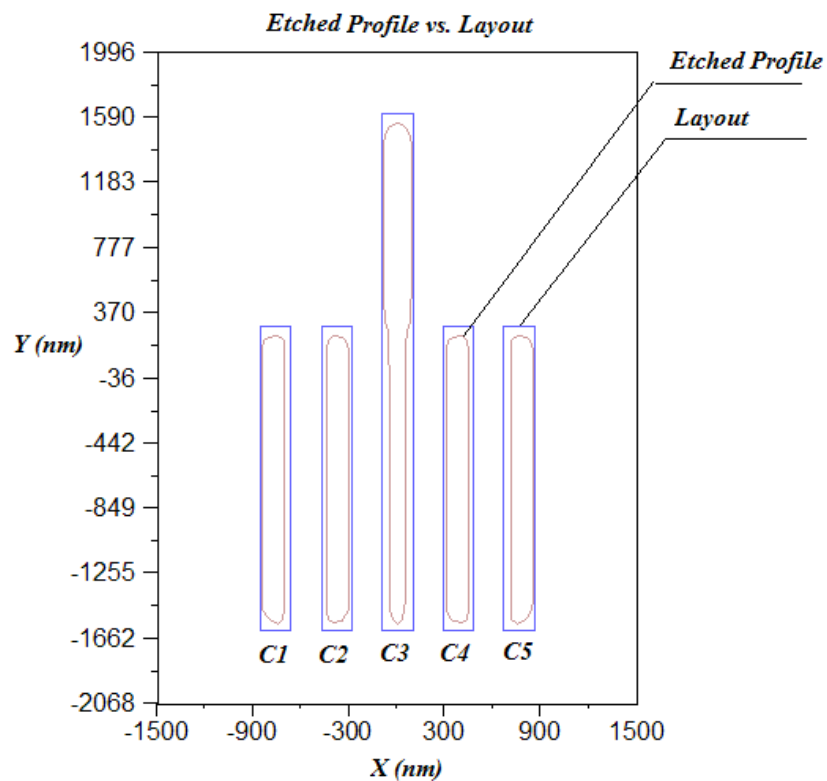


Figure 3. An example of etch profile vs. layout (top view)

The traditional LPE methodology is shown in Figure 2. First, the basic interconnect structure and the specific technology files are input to the 2D/3D field solver. The solver generates a pattern library to be used for parasitic extraction. Second, LPE tools read the layout file and this pattern library to extract the parasitics (RLC) of the circuits. This methodology does not consider process variations and lithography effects, and as a result, impacts the accuracy of the extracted parasitics. As an example, Figure 3 shows the top view of the layout and etched profile of a five bar structure. The lithography results are simulated by PROLITH. It is shown that the difference between two profiles is

significant, especially around the corners; meanwhile, the pattern of interconnect structure also affects the etched profile. As in this case, conductor C3 has a relative narrower size on the bottom part compared with the size on the top. The extracted errors of traditional parasitic extraction results are shown in Table 1. In this table, the maximum errors can reach as high as 20%. The 3D field solver we used is FastCap [5], which is academic software for computing the self and coupling capacitances of a conductive 3D structure.

Table 1. Parasitic Capacitance for Example Shown in Figure 3

Capacitance	Capacitance of Etched Conductor (aF)	Capacitance of Layout Conductor (aF)	Error
Self Cap. C1	71.06	81.08	14.10%
Self Cap. C2	96.51	114.30	18.43%
Self Cap. C3	125.00	143.00	14.40%
Self Cap. C4	96.26	114.10	18.53%
Self Cap. C5	71.14	81.07	13.96%
Coupling Cap. C12	40.30	48.32	19.90%
Coupling Cap. C13	7.62	7.85	3.02%
Coupling Cap. C14	2.08	2.16	3.85%
Coupling Cap. C15	2.27	2.34	3.08%
Coupling Cap. C23	42.09	50.71	20.48%
Coupling Cap. C24	3.00	3.03	1.00%
Coupling Cap. C25	2.03	2.07	1.97%
Coupling Cap. C34	41.86	50.52	20.69%
Coupling Cap. C35	7.78	8.01	2.96%
Coupling Cap. C45	40.25	48.25	19.88%

This paper proposes a new LPE strategy considering lithography effects and process variations as the interconnect structures are given. This strategy corrects the original pattern library based on the lithography simulation results. The new pattern library is used to do the shape transformation for the input structures gotten from the circuit layout. After the shape transformation is done, the LPE tools extract the parasitics and generate the circuit model for SPICE simulation. This paper also studies the impacts of the mask critical dimension (CD) variations on parasitic extraction. For different interconnect structures, the capacitance and resistance variations are studied and illustrated.

The rest of the paper is organized as follows: In Section 2, the lithography simulation tool is introduced. Section 3 proposes the new LPE strategy that will consider the process variation and lithography effects. In Section 4, the effects of mask variations on parasitic extraction are studied. Finally, in Section 5, we conclude our research results.

2. LITHOGRAPHY SIMULATION AND PARASITIC EXTRACTION

Optical lithography is one of the major components in semiconductor manufacturing process and has great effects on the final device and circuit performance. With the development of optical lithography techniques, it is possible to make smaller and smaller features on the wafer so that the performance of the circuit can be continuously improved. To better study the lithography process, the lithography modeling and simulation have been introduced into industry implementation for about 30 years. Due to its speed and cost-effectiveness, lithography simulation has been widely used to study the process development, determination of sensitivity to manufacture variables, mask design verification and yield analysis [6][7][8]. Modern lithography simulation engine can provide accurate process models for the current lithography sequence. In this paper, we use 3D lithography simulator PROLITH version 8.1.2 to study the process and mask variations and their effects on parasitic extraction. In our experiments, 90-nm technology is used and 193-nm UV light is assumed as the lithographic light source.

The experiments performed in this paper involve several steps: 1. Selection of the masks from the design or the interconnect library. 2. Determination of the process window and optimization of the manufacture parameters. 3. Lithography simulation and the post-process of simulation results. 4. Parasitic extraction of the simulation results. The

details of these steps are introduced as follows.

To study the lithography and process variation effects on interconnect parasitics, we need to select proper masks for simulation. As this paper concentrates on interconnect parasitic extraction problem, we select the masks based on Raphael™ interconnect library and PROLITH mask database. Raphael™ is a product of Synopsys to provide a collection of 2D and 3D field solvers and interfaces that can be used to obtain accurate interconnect models. This software package is designed to simulate the complex on-chip interconnect structures. Additionally, Raphael™ provides an interconnect library which is composed of many typical geometries that represent common interconnect structures used in the layout design, such as vias, pads and arrays of parallel traces [9].

After the mask is selected, the proper lithography parameters need to be selected. In the lithography process, there are several important parameters need to be determined to achieve the optimized exposure and lithography results. Among them, the choices of resist thickness, exposure dose and the effects of focus are critical for the quality control of lithography process simulation. We follow the set simulation method provided by PROLITH to select the optimal parameters and process windows [10].

The flow of our simulation experiments is shown in Figure 4. First, the typical structures are selected from the Raphael™ interconnect library and PROLITH. These structures consist of both 2D and 3D interconnect patterns. Second, the masks with OPC are derived for lithography simulation. Based on the masks and proper processing parameters selected, the lithography simulation by PROLITH is carried out to produce the final 3D geometry of different interconnect structures. Finally, the lithography images can be read and post-processed by user defined PROLITH program interface (PPI) functions. Meanwhile, the input files for the field solver to extract the parasitics are generated.

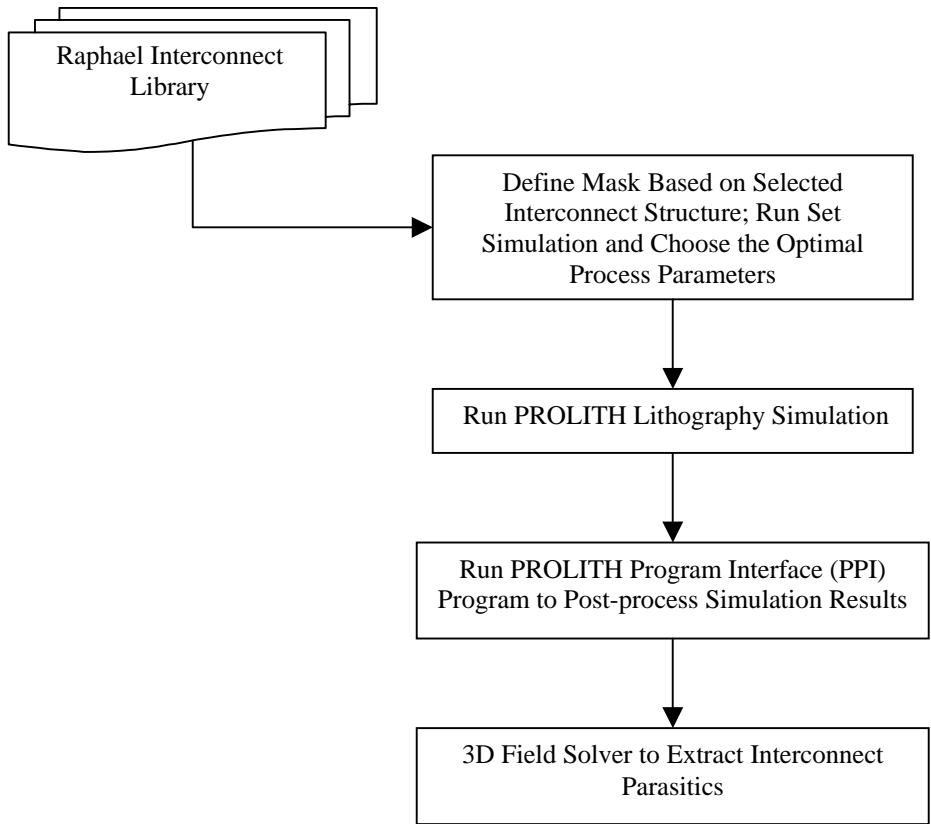


Figure 4. Simulation and Experimental Setup

3. LPE STRATEGY CONSIDERING LITHOGRAPHY EFFECTS

As we mentioned in Section 1, traditional LPE strategy does not consider the lithography effects, and the error of the extraction results can reach as high as 20%. Although people can simulate the fabrication process for the whole circuit and then extract the parasitics from the simulation results, it is very time consuming, especially for large integrated circuit. Therefore, new technologies are needed to extract the parasitics efficiently and precisely.

In this section, we propose a new strategy to improve the accuracy of parasitic extraction, which is consistent with the traditional parasitic extraction flow. The strategy is shown in Figure 5. The difference between this new strategy and the traditional one shown in Figure 2 is that a shape correction step based on the lithography simulation is inserted into the pattern library generation process. The shape correction includes three major steps: corner correction, sidewall correction and 3D shape construction. In corner correction, each corner of the conductor is linearly interpolated to approximate the etched profile. In sidewall correction, the cross section of the lithography result is approximated by a trapezoid, and the average sidewall angle is computed from the lithography simulations. In 3D construction, as the bottom plane shape of the conductor is formed by using the corner correction to the original interconnect structure, a 3D conductor is constructed by scaling the bottom plane based on the sidewall correction.

The shape correction is performed for all the interconnect structures commonly used in the layout (such as the ones used in the Raphael™ interconnect library). These corrected shapes are input to the 2D/3D field solver. A pattern library is formed to support the LPE tools. Finally, the LPE tool extracts the parasitics from circuit layout.

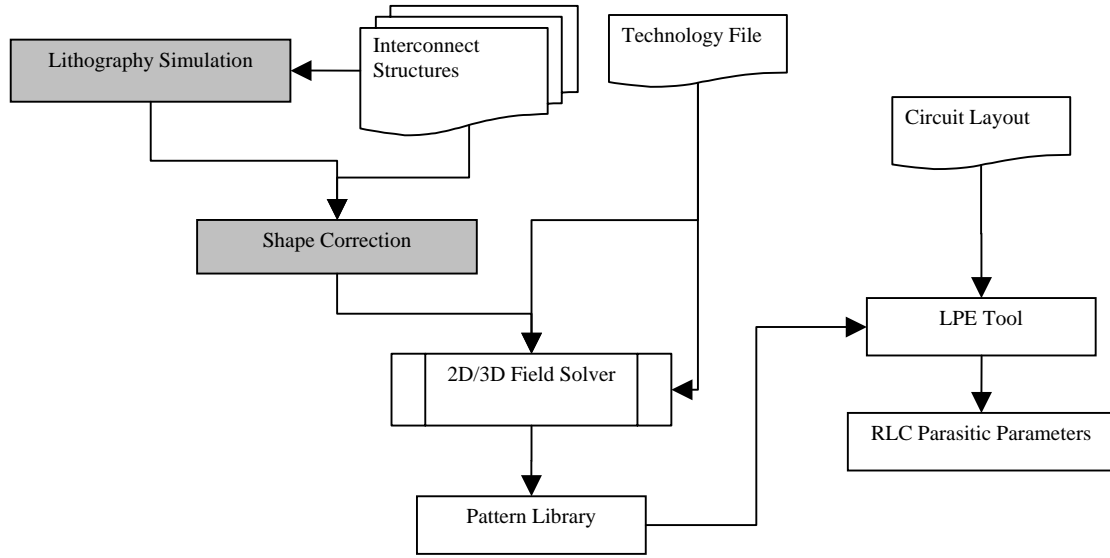


Figure 5. Proposed LPE Strategy

For resistance extraction, as the etched profile is not a regular geometry, we use the cross section area and the length of the shape corrected conductor to estimate the resistance. Consider a 3D isolated conductor shown in Figure 6. Ideally, the conductor should be a cuboid with height H_1 and width W_1 , as shown in cross section view M-M'. However, the cross section of the actual fabricated geometry will be more like a trapezoid, as shown as the cross section view K-K' in Figure 6, we can estimate the actual resistance of the conductor by the following classic formula:

$$R = \rho \frac{L}{S} = \rho \frac{L}{\frac{A+B}{2} H_2} = \rho \frac{2L}{(A+B)H_2} ,$$

where ρ is the resistivity, L and S are the length and the cross section area of the conductor, respectively. For every simulated interconnect structure, we can estimate the conductor's resistance with the cross section shape and the length of the conductor, which can be obtained directly from the lithography simulation output.

Table 2 shows the result of the extracted parasitic capacitance of conductor after lithography simulation and the corrected shape conductor, respectively; this result is based on the example structure shown in Figure 3. Compared with the traditional extraction results shown in Table 1, the error of capacitance extraction is reduced from 20% to 2%.

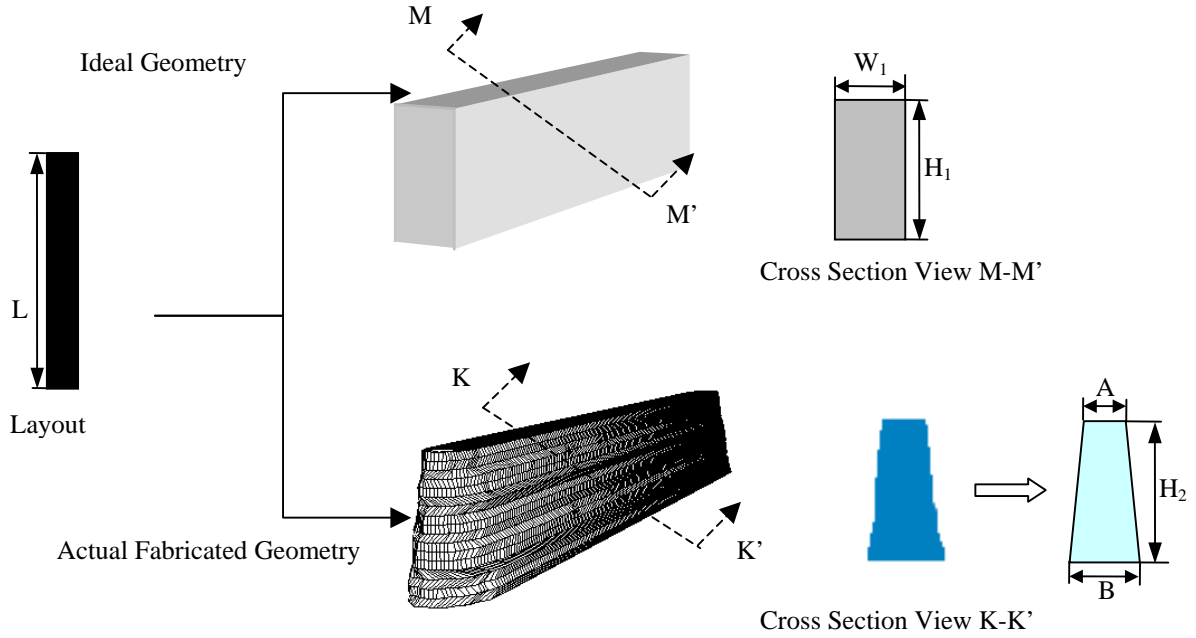


Figure 6. Interconnect Structure Resistance Estimation

Table 2. Parasitic Capacitance for Example Shown in Figure 3 Using New LPE Strategy

Capacitance	Capacitance of Etched Conductor (aF)	Capacitance of Shape Corrected Conductor (aF)	Error
Self Cap. C1	71.06	69.92	1.60%
Self Cap. C2	96.51	95.39	1.16%
Self Cap. C3	125.00	127.40	-1.92%
Self Cap. C4	96.26	94.30	2.04%
Self Cap. C5	71.14	70.10	1.46%
Coupling Cap. C12	40.30	39.60	1.74%
Coupling Cap. C13	7.62	7.73	-1.44%
Coupling Cap. C14	2.08	2.04	1.92%
Coupling Cap. C15	2.27	2.23	1.76%
Coupling Cap. C23	42.09	41.92	0.40%
Coupling Cap. C24	3.00	3.02	-0.67%
Coupling Cap. C25	2.03	2.02	0.49%
Coupling Cap. C34	41.86	41.67	0.45%
Coupling Cap. C35	7.78	7.64	1.80%
Coupling Cap. C45	40.25	39.50	1.86%

4. MASK VARIATION EFFECTS ON INTERCONNECT PARASITICS

As a result of shrinking size of the semiconductor device in recent years, the requirements for advanced photomask are getting more stringent. In addition, phase shifting mask (PSM) and optical proximity correction (OPC) technologies also require the cost effective and high quality masks. These requirements have added the new challenges for mask fabrication. Currently, important issue includes the control of the uniformity of mask CD, and the mask industry is still seeking good mask fabrication techniques to get a better control over the CD variation and reduction of the defect. With the smaller feature size, a very small variation on the mask could actually generate a relatively huge impact on the printed results on wafer. Therefore, the study of the circuit performance under mask variation is becoming a more important problem in design for manufacturing (DFM) and should get enough attention for the circuit designers.

To investigate the behavior of mask variations on parasitic extraction, we follow the experiments described in Section 2. In our experiment, we use 90-nm technology; the nominal mask CD value is 250nm and variation of the mask CD changes within $\pm 10\%$ of the nominal value ($\pm 25\text{nm}$). The simulation is carried out and parasitic capacitance and resistance are extracted. The 3D field solver we used is FastCap. The input file for FastCap is generated by using the PROLITH program interface and consists of discretized conductor surfaces in form of triangular or quadrangular panels in 3D space. The results are provided as a capacitance matrix that includes both the self and coupling capacitance.

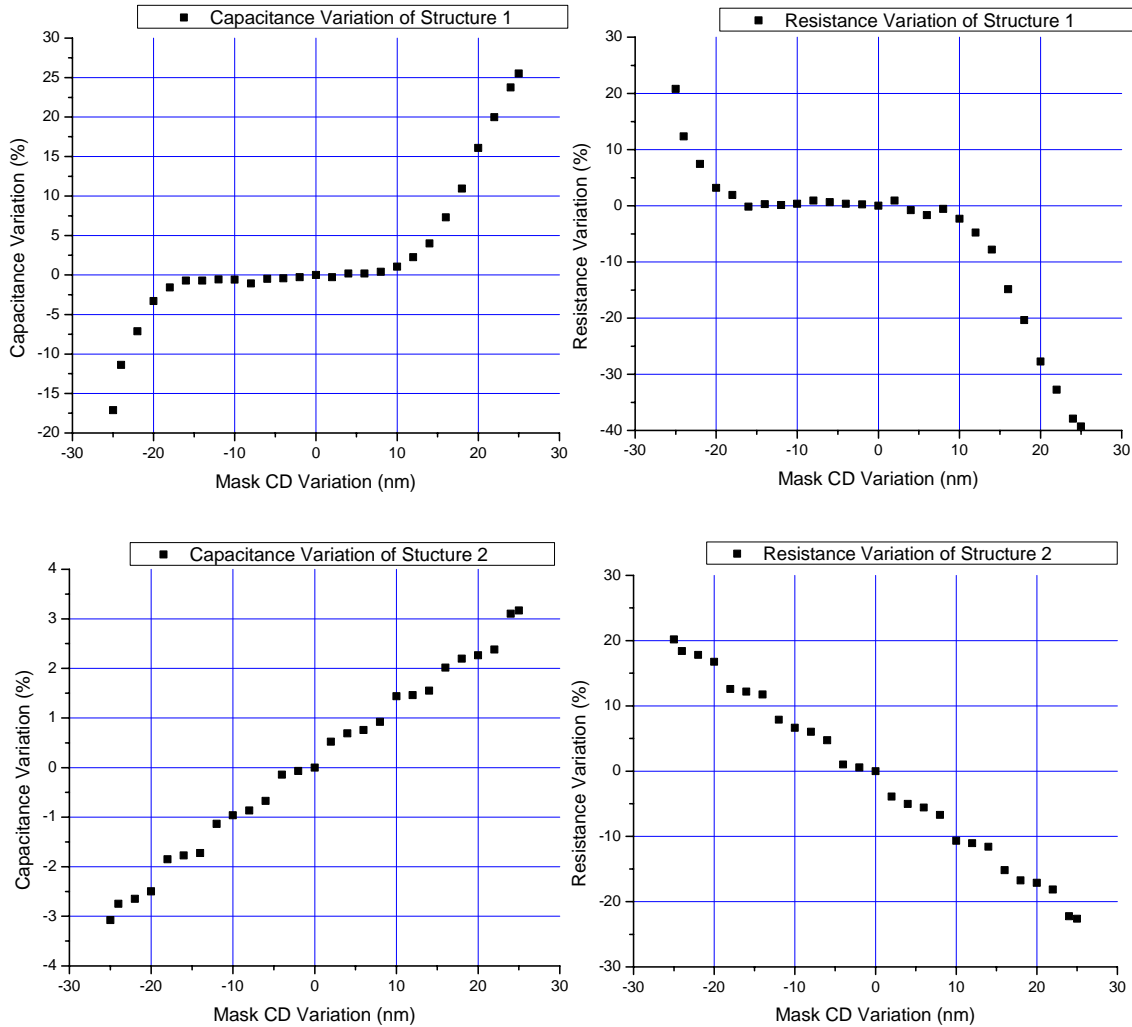


Figure 7. Mask CD Variation Impact on Parasitic Parameters

Experimental results of two interconnect structures are shown in Figure 7. Structure 1 includes two conductors in denser pattern while structure 2 has only one isolated conductor. With the increasing of the mask CD size, the capacitance is increasing while the resistance is decreasing because of the increase of the crossing area. The capacitance variation of structure 1 is from -12.5% to 17.5%, while the resistance variation of this structure is from -35% to 35%. For structure 2, the capacitance variation is very small (from -5% to 5%), while the resistance variation is similar to structure 1. These figures show how the mask variation affects the interconnect parasitics. More interconnect structures are studied in a similar way and the results are illustrated in the appendix.

From the results shown in Figure 7 and Appendix, we can conclude that depending on the interconnect structure, the capacitance variation changes from $\pm 5\%$ to $\pm 25\%$; while the resistance variation is around $\pm 30\%$. Meanwhile, the variation of most structures shows a nonlinear curve as the mask CD varies. This nonlinearity is partly because that the etched feature size varies when the mask CD varies, this variation is not a linear function for many reasons, such as thin-film interference effect, the defocus effect and the vibrations, etc. [10]. Also, the nonlinearity is pattern and density dependent; the parasitic capacitances of different patterns behave differently as the mask varies. With this approach, circuit designers can predict the impacts of mask CD variations on parasitics for different structures, thus further study the performance of the circuit under the mask variations.

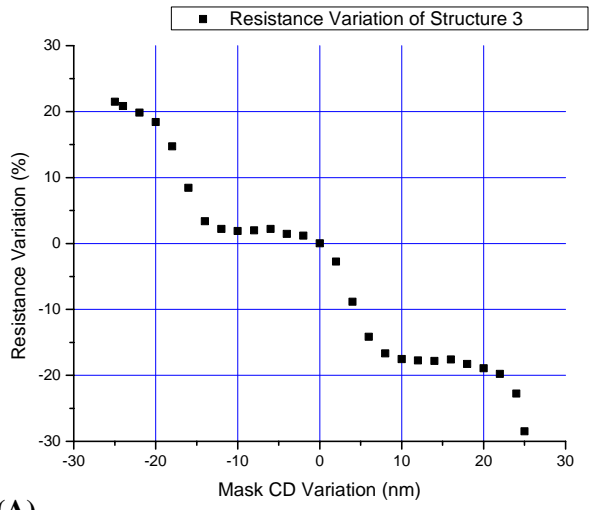
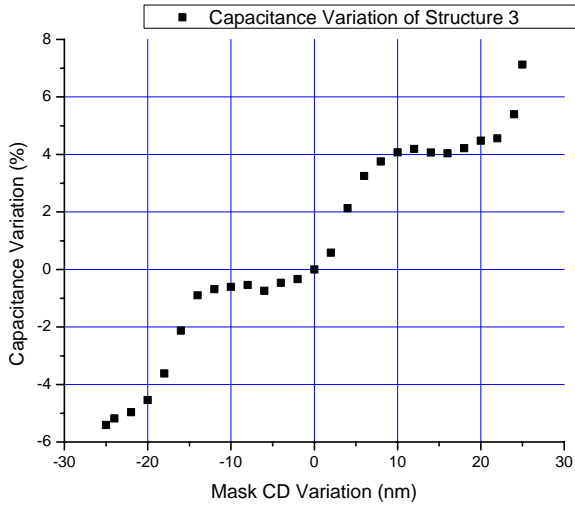
5. CONCLUSIONS

Based on the lithography simulation, this paper proposes a shape correction method to adjust the interconnect structure for LPE tools. Compared with the existing extraction strategy, this extraction method has a higher accuracy. This strategy can be implanted into the current design flow with minimum change. Meanwhile, this paper studies the impacts of the mask variability on interconnect capacitance and resistance extraction, the variability analysis is based on PROLITH lithography simulation and is tested on the typical interconnect structures constructed from RAPHAELTM interconnect library and PROLITH mask database. The analysis approach is useful to study how the mask variation will affect the interconnect parasitics and can be used for circuit designers to study the performance of the circuit under the mask variations.

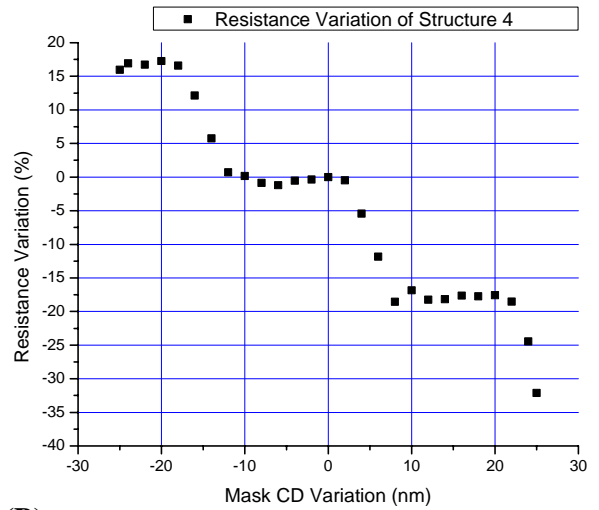
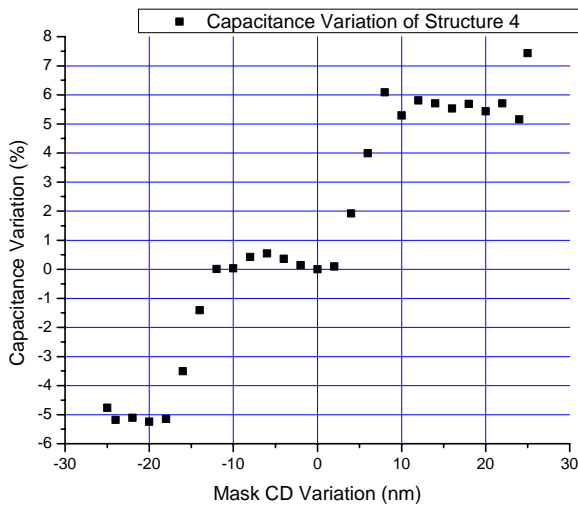
6. REFERENCES

- [1] P. Zarkesh-Ha and J.D. Meindl, "Optimum chip clock distribution networks", Proceedings of the IEEE 2001 International Interconnect Technology Conference, 1999, pp. 18 – 20.
- [2] V. Mehrotra, S. L. Sam, D. Boning, A. Chandrakasan, R. Vallishayee and S. Nassif, "A methodology for modeling the effects of systematic within-die interconnect and device variation on circuit performance", Proceedings of DAC, 2000, pp. 172-175.
- [3] V. Mehrotra and D. Boning, "Technology scaling impact of variation on clock skew and interconnect delay", Proceedings of the IEEE 2001 International Interconnect Technology Conference, 2001, pp. 122 – 124.
- [4] ITRS, "The International Technology Roadmap for Semiconductors: 2004 update", <http://www.itrs.net/Common/2004Update/2004Update.htm>.
- [5] K. Nabors, J. White, "FastCap: A Multipole Accelerated 3-D Capacitance Extraction Program", IEEE Trans. CAD, Vol. 10, No. 11 (1991), pp. 1447–1459.
- [6] P. M. Mahoney and C. A. Mack, "Cost Analysis of Lithographic Characterization: An Overview", Optical/Laser Microlithography VI, Proc., SPIE Vol. 1927 (1993) pp. 827-832.
- [7] J. Kasahara, M. V. Dusa, and T. Perera, "Evaluation of a Photoresist Process for 0.75 Micron, G-line Lithography", Proc., SPIE Vol. 1463 (1991) pp. 492-503.
- [8] Chris A. Mack, "Lithography Simulation in Semiconductor Manufacturing", Proc., SPIE Vol. 5645-7 (2004). pp.63-83.
- [9] <http://www.synopsys.com/>.
- [10] Chris A. Mack, Inside Prolith : A Comprehensive Guide to Optical Lithography Simulation, Finle Technologies Inc., 1997.

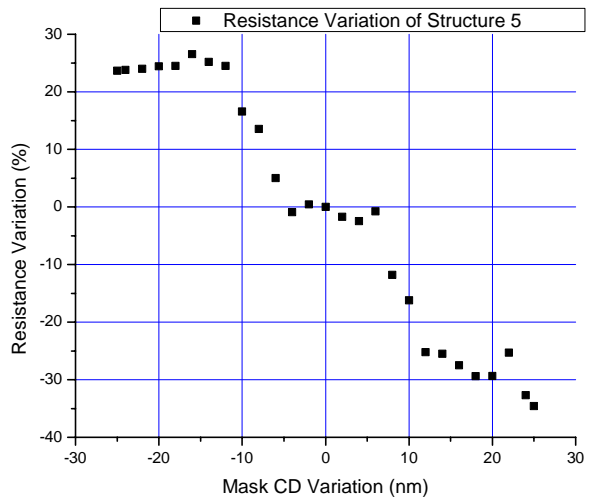
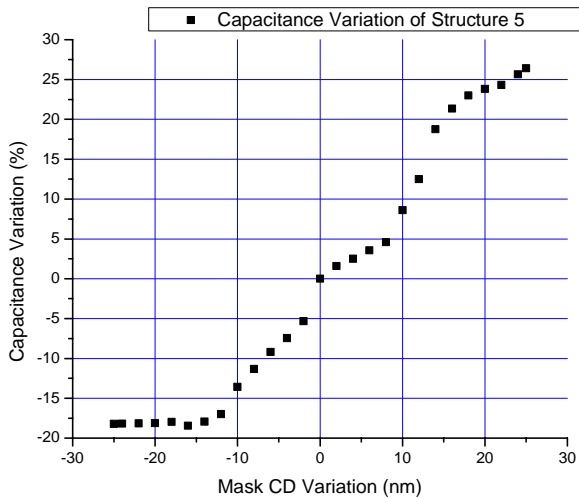
APPENDIX: Mask Variation Impact on Parasitics for Different Interconnect Structures



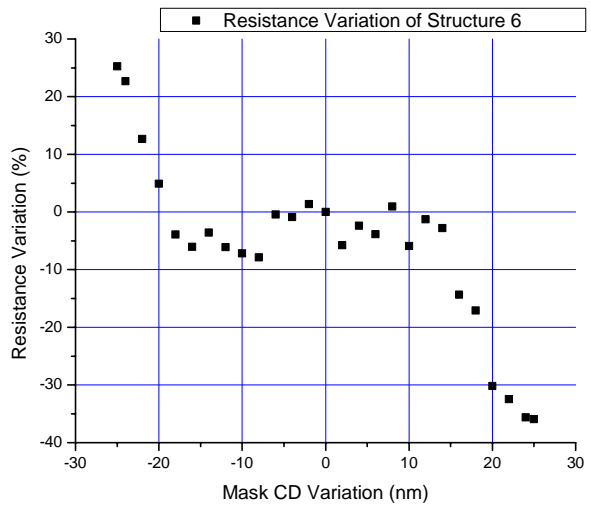
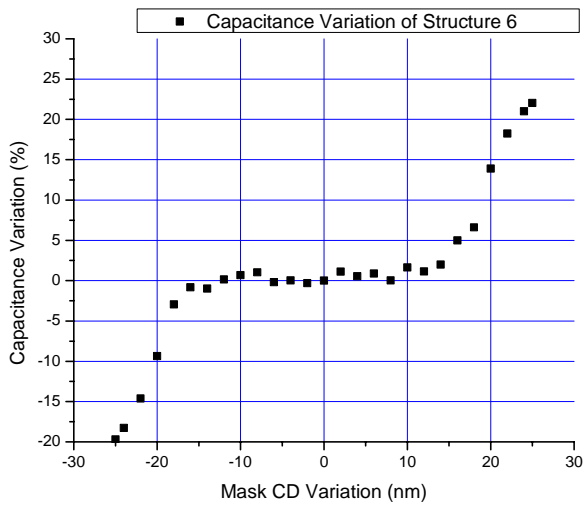
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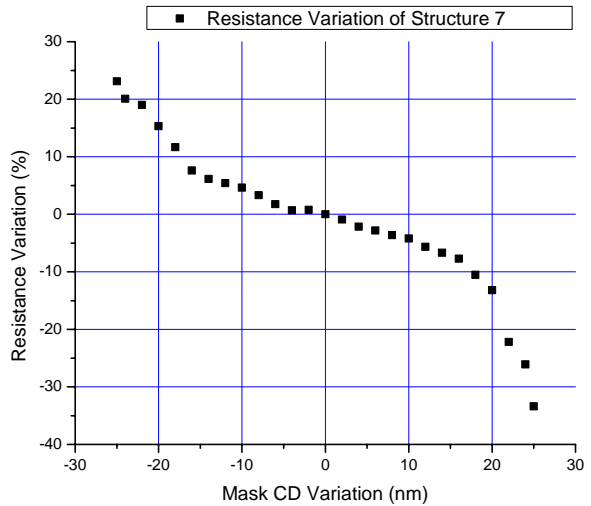
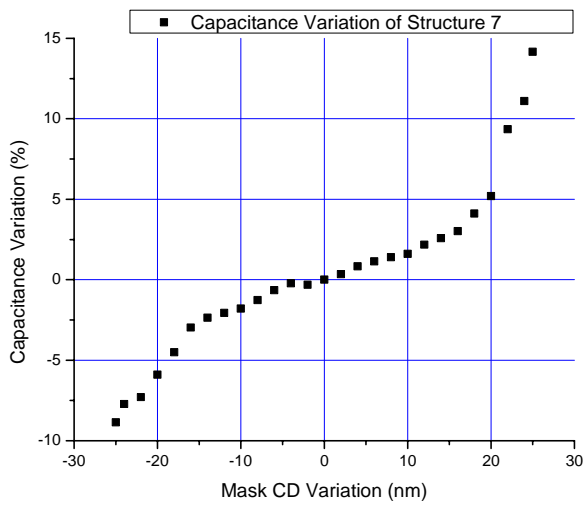
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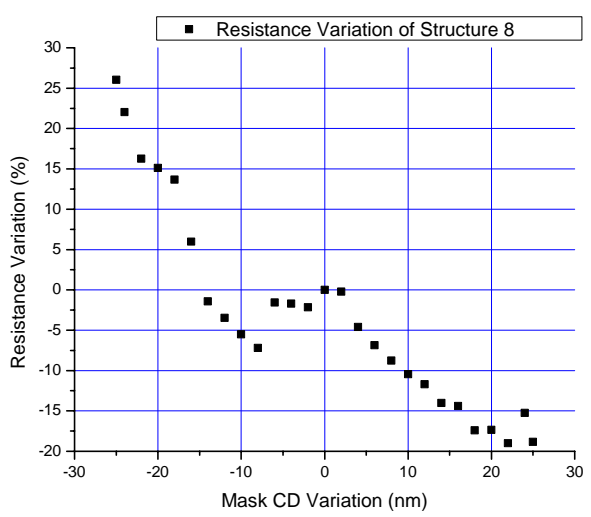
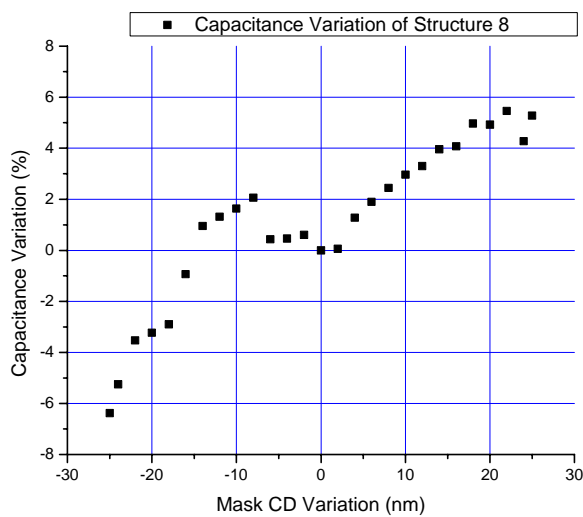
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(D)



(E)



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